REMARKS

The Office Action mailed on November 5, 2002, has been received and reviewed.

Claims 1 through 9, 11 through 14, and 16 through 21 are currently pending in the above-referenced application, each standing rejected.

Claims 10 and 15 have been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1, 5 through 9, 12 through 14, 17, and 18 through 21 stand rejected under 35 U.S.C. § 102.

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Akram

Claims 1, 5 through 9, 12, 17, 18, 20 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,072,236 to Akram et al. (hereinafter "Akram").

Akram describes an embodiment, among the descriptions of various embodiments therein, micromachined chip scale packages that include semiconductor dice with silicon blanks laminated to the surfaces thereof. As an alternative to silicon, the blanks may be formed from ceramic or mullites. Col. 5, lines 48-51. Each blank includes apertures through which bond pads of the semiconductor die are exposed. *See, e.g.,* FIGs. 6-8. Additionally, trenches may be formed from one or more apertures to an edge of the silicon blank and a corresponding edge of the semiconductor die. *See* FIGs. 6-8; col. 6, lines 32-67.

Claim 1, as amended and presented herein, recites a semiconductor device that includes at least one bond pad of a surface of a semiconductor die adjacent an edge thereof and a layer comprising at least one polymer on at least a portion of a surface of the semiconductor die.

Amended independent claim 1 also recites that the layer includes a notch formed therein. The at least one bond pad of the semiconductor die is exposed through the notch, which includes a portion that extends completely through the layer and which is continuous with an edge of the layer.

By way of contrast with amended independent claim 1, Akram lacks any express or inherent description that the blank thereof may include one or more polymers. Instead, the description of Akram is to a blank which is formed from the same material as a semiconductor die over which it is to be positioned (*e.g.*, silicon, gallium arsenide, etc.), ceramic, or a mullite. Col. 5, lines 48-51. Therefore, Akram does not and cannot anticipate each and every element of amended independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e).

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), amended independent claim 1 is allowable.

Claims 5 through 9 are each allowable, among other reasons, as depending either directly or indirectly from amended independent claim 1, which is allowable.

<u>Yunoki</u>

Claims 12 through 14 and 18 through 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yunoki et al., U.S. Patent 5,236,372. Applicants respectfully traverse this rejection, as hereinafter set forth.

Yunoki describes a printed circuit board which is configured for no-insertion force, or zero-insertion force, with a larger-scale substrate. Among other things, that printed circuit board includes an insulating layer 34 on a surface thereof. FIG. 2; col. 5, lines 23-27. The insulating layer 34 includes notches 35 through which contact terminals 32, 33 are exposed. *Id.* The edge of the insulating layer 34 and the edges of the notches 35 may be beveled. *See, e.g.,* FIG. 2; col. 5, line 63, to col. 6, line 9. Yunoki is silent as to the type of material from which the insulating layer 34 may be formed.

Independent claim 12, as amended and presented herein, recites a protective layer for a semiconductor die. The protective layer includes a substantially planar member that comprises polymer. In addition, the protective layer includes at least one notch formed adjacent an edge of

the substantially planar member. The at least one notch is configured to expose at least a portion of a corresponding bond pad of the semiconductor die upon being positioned over an active surface of the semiconductor die.

Yunoki neither expressly nor inherently describes that the insulating layer 34 thereof is configured for assembly with a semiconductor die or that the insulating layer 34 may include a substantially planar member that comprises polymer, as recited in amended independent claim 12. Therefore, it is respectfully submitted that Yunoki does not and cannot anticipate each and every element of amended independent claim 12, as required under 35 U.S.C. § 102(b).

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 12 is allowable.

Each of claims 13, 14, and 18 through 21 is allowable, among other reasons, as depending either directly or indirectly from amended independent claim 12, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102 rejections of claims 1, 5 through 9, 12 through 14, 17, and 18 through 21 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 1 through 4, 6 through 11, 15, and 16 stand rejected under 35 U.S.C. § 103(a). Applicant submits that M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Yunoki

Claims 1, 4, and 6 through 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yunoki.

The relevant teachings or suggestions of Yunoki have been summarized above.

It is respectfully submitted that there are at least two reasons that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) cannot be established against any of claims 1, 4, or 6 through 9 based on the teachings or suggestions of Yunoki.

First, it is respectfully submitted that one or ordinary skill in the art would not have been motivated to modify the teachings of Yunoki in such a way as to render the subject matter recited in independent claim 1, as amended herein, or any of claims 4 or 6 through 9, which depend from independent claim 1, unpatentable. In particular, one of ordinary skill in the art would not have been motivated to apply Yunoki's teaching of an insulative layer for a printed circuit board to a semiconductor die, as recited in amended independent claim 1.

Second, at the least, Yunoki does not teach or suggest each and every element of amended independent claim 1. Specifically, as its teachings are drawn to printed circuit boards, Yunoki lacks any teaching or suggestion that the insulating layer 34 thereof may be positioned upon a surface of a semiconductor die. Yunoki also lacks any teaching or suggestion that the insulating layer 34 thereof may comprise polymer.

As Yunoki does not teach or suggest each and every element of amended independent claim 1, it cannot teach or suggest each and every element of any of claims 4 or 6 through 9, each of which depends either directly or indirectly from amended independent claim 1.

For these reasons, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been set forth against any of claims 1, 4, or 6 through 10. Thus, under 35 U.S.C. § 103(a), each of these claims is allowable.

Yunoki in View of Kniese

Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yunoki, in view of U.S. Patent 4,806,103 to Kniese et al. (hereinafter "Kniese").

Claims 2 and 3 are both allowable, among other reasons, as respectively depending directly and indirectly from amended independent claim 1, which is allowable.

Moreover, it is respectfully submitted that the teachings or suggestions of Yunoki and Kniese, either individually or in any combination thereof, do not support a *prima facie* case of obviousness under 35 U.S.C. § 103(a) against either claim 2 or claim 3. In particular, one of ordinary skill in the art would not have been motivated by either these references or the knowledge that was generally available in the art before the priority date of the above referenced application to combine the teachings of these references in such a way as to render the subject matter recited in claim 2 or claim 3 unpatentable. This is because both Yunoki and Kniese are drawn to structures that are used to facilitate edge connection of printed circuit boards to larger-scale substrates (*e.g.*, motherboards) rather than to structures that are useful with semiconductor dice, as recited in amended independent claim 1, from which claims 2 and 3 depend.

Accordingly, under 35 U.S.C. § 103(a), claims 2 and 3 are both allowable.

<u>Yunoki, in View of Dines and Lee</u>

Claims 10, 11, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yunoki, in view of U.S. Patent 4,303,291 to Dines (hereinafter "Dines") and U.S. Patent 5,386,087 to Lee et al. (hereinafter "Lee").

Claims 10 and 15 have been canceled without prejudice or disclaimer, rendering the rejections thereof moot.

Claims 11 and 16 are both allowable, among other reasons, as depending either directly or indirectly from amended independent claims 1 and 12, respectively, which are allowable.

Additionally, it is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established since one of ordinary skill in the art would not be motivated to combine the teachings of Yunoki, Dines, and Lee in such a way as to render unpatentable the subject matter to which claims 11 and 16 are directed.

Independent claim 1, as amended herein, is drawn to a semiconductor device that includes, among other things, a semiconductor die and a layer comprising polymer on at least a portion of a surface of the semiconductor die. Amended independent claim 12 is drawn to a

protective layer for a semiconductor die that includes a substantially planar member comprising polymer.

The teachings or suggestions of Yunoki, Dines, and Lee are each limited to structures, including insulating layers and edge connect structures, that are useful with printed circuit boards. As none of Yunoki, Dines, or Lee or any combination of such cited prior art teaches or suggests a layer which is useful with a semiconductor die, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by the teachings of any of these references, taken either separately or together, to combine them in such a way as to render either claim 11 or claim 16 obvious and, thus, unpatentable under 35 U.S.C. § 103(a).

Therefore, under 35 U.S.C. § 103(a) claims 11 and 16 are both allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1 through 4, 6 through 11, 15, and 16 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1 through 9, 11 through 14, and 16 through 21 is allowable. An early notice of the allowability of each of these claims, as well as an indication that the above-referenced application has been passed for issuance, are respectfully solicited. If any issues preventing the allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A semiconductor device, comprising:

at least one [contact] bond pad positioned on a surface of [the] a semiconductor device adjacent an edge thereof; and

a layer comprising [dielectric material] polymer on at least a portion of said surface, said layer having a notch formed therein which exposes at least a portion of said at least one [contact] bond pad.

2. (Amended) The semiconductor device of claim 1, wherein an edge portion of said layer adjacent said edge of [the] said semiconductor [device] die tapers from a surface of said layer toward said edge of [the] said semiconductor [device] die.

4. (Twice amended) The semiconductor device of claim 1, wherein said notch is tapered from a surface of said layer toward said surface of [the] said semiconductor [device] die.

6. (Twice amended) The semiconductor device of claim 1, wherein said notch substantially surrounds said at least one [contact] bond pad.

7. (Amended) The semiconductor device of claim 1, including a plurality of [contact] bond pads.

8. (Amended) The semiconductor device of claim 7, wherein at least some of said [contact] bond pads are located adjacent said edge.

9. (Amended) The semiconductor device of claim 8, wherein said layer includes regions extending laterally between adjacent [contact] bond pads of said at least some [contact] bond pads.

11. (Amended) The semiconductor device of claim 1, wherein said [dielectric material] polymer comprises a photoimageable material.

12. (Amended) A protective layer for a semiconductor [device] die, comprising:
a substantially planar member comprising [dielectric material] polymer; and
at least one notch formed adjacent an edge of said substantially planar member, said at least one notch being configured to expose at least a portion of a corresponding [contact] bond pad of the semiconductor [device] die upon positioning the protective layer over [a] an active surface of the semiconductor [device] die.

16. (Amended) The protective layer of claim 12, wherein said [dielectric material] polymer comprises a photoimageable material.

18. (Amended) The protective layer of claim 12, wherein said substantially planar member is configured to substantially cover [a] said active surface of the semiconductor [device] die upon assembly therewith.

19. (Twice amended) The protective layer of claim 12, wherein said substantially planar member is configured to cover only a portion of a surface of the semiconductor [device] die adjacent an edge thereof proximate to which at least one [contact] bond pad is located upon assembly of the protective layer with the semiconductor [device] die.

21. (Twice amended) The protective layer of claim 12, wherein said at least one notch is configured to substantially surround the corresponding [contact] bond pad upon assembly of the protective layer with the semiconductor device.